Static Analysis by Abstract Interpretation of Functional Properties of Device Drivers in TinyOS

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Workshop on Static Analysis of Concurrent Software
September 11th, 2016
Edinburgh, Scotland
Part I

Context
We target programs for wireless sensor networks (WSN).

A distributed system of wirelessly connected embedded nodes for monitoring a physical phenomena.

Ad hoc communications and collaborative routing.

Many applications: irrigation, weather/pollution monitoring, fire detection, etc.
We aim at verifying the correctness of device drivers in TinyOS programs.

Motivation

Drivers difficult to develop/debug, error-prone and critical.

Summary of Our Approach

- We focus on functional properties specifying programming rules to access hardware correctly.
- We employ Abstract Interpretation to automatically verify that all possible executions obey such specifications.

For more details:
Static Analysis by Abstract Interpretation of Functional Properties of Device Drivers in TinyOS

Part II

Expressing Specifications
Specifications
Example: ATmega128 Timer/Counter0

Rule
If Timer/Counter0 is used to wake the device up... precautions must be taken...

1. Write a value to TCCR0, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.

Formalism
To formalize this rule, we use an automaton tailored to describe patterns of hardware interactions.
Specifications
Example: ATmega128 Timer/Counter0

ATmega128

- When writing to one of the registers TCCR0, OCR0, or TCGR0, the value is transferred to a temporary register, and latched after two positive edges on TOSS1. The user should not write a new value before the contents of the temporary register have been transferred to its destination. Each of the three mentioned registers have their individual temporary registers.
- If Timer/Counter0 is used to wake the device up, precautions must be taken to ensure that the device never enters power-save or extended standby mode before the OCR0 value has been written to the temporary register. The Interrupt Flag should be set before writing to the Timer/Counter0 registers.

Formalism
To formalize this rule, we use an automaton tailored to describe patterns of hardware interactions:

1. Write a value to TCCR0, OCR0, or TCGR0.
2. Wait until the corresponding Update Busy Flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby modes.

When the asynchronous operation is selected, the 32.768kHz Oscillator for Timer/Counter0 is always running, except in Power-down and Standby modes. After a Power-up Reset or wake-up from Power-down or Standby mode, the user should be aware of the fact that the Oscillator might take as long as one second to stabilize. The user is advised to wait for at least one second before using Timer/Counter0 after power-up or wake-up from Power-down or Standby mode. The contents of all Timer/Counter0 Registers must be considered lost after a wake-up from Power-down or Standby mode due to unreliable clock signal upon start-up, no matter whether the Oscillator is in use or a clock signal is applied to the TOS1 pin.

Description of wake-up from Power-save or Extended Standby mode when the timer is clocked asynchronously. When the interrupt condition is real, the wake-up process is started on the following cycle of the timer clock, that is, the timer is always awakened by at least one cycle before the processor can read the counter value. After wake-up, the MCU is halted for four cycles, it executes the interrupt routine, and resumes execution from the instruction following SLEEP.

Reading of the TOSS1 Register shortly after wake-up from Power-save mode may give an incorrect result. Since TOSS1 is clocked on the asynchronous TOS1 clock, reading TOSS1 must be done through a register synchronized to the internal IC clock domain. Synchronization takes place for every rising TOS1 edge. When waking up from Power-save mode, and the IC clock (fIC) is again becomes active, TOSS1 will read as the previous value (before entering sleep) until the next rising TOS1 edge. The phase of the TOS1 clock after waking up from Power-save mode is essentially unpredictable, so it depends on the wake-up time. The recommended procedure for reading TOSS1 is thus as follows:
1. Write any value to either of the registers OCR0 or TCGR0.
2. Wait for the corresponding Update Busy Flag to be cleared.
3. Read TOSS1.
If Timer/Counter0 is used to wake the device up [...], precautions must be taken [...]

1. Write a value to TCCR0, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.
If Timer/Counter0 is used to wake the device up [...], precautions must be taken [...]

1. Write a value to TCCR0, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
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**Formalism**

To formalize this rule, we use an automaton tailored to describe patterns of hardware interactions.
An abstract device property is a special register automaton describing patterns of hardware interactions:

$$A = (S, s_0, s_{\text{BUG}}, \mathcal{R}, \xi, \mathcal{T})$$

where:
- $S$ set of states
- $s_0$ initial state
- $s_{\text{BUG}}$ bug state
- $\mathcal{R}$ set of hardware registers
- $\xi = \{X^\diamond \mid X \in \mathcal{R}, \diamond \in \{r, w\}\} \cup \{\text{int}_i \mid i \in \mathbb{N}\} \cup \{\alpha, \text{sleep}\}$
- $\mathcal{T} \subseteq S \times \xi \times S \times Stmt_C \times Stmt_C$
If Timer/Counter0 is used to wake the device up [...] precautions must be taken [...]

1. Write a value to TCCR0, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.

When writing to one of the registers TCNT0, OCR0, or TCCR0, the value is transferred to a temporary register and latched after two positive edges on TOCKI. The user should not write a new value before the contents of the Temporary Register have been transferred to its destination. Each of the three mentioned registers have their own individual temporary register, which means that e.g., writing to TCNT0 does not disturb an OCR0 write in progress. To detect that a transfer to the destination register has taken place, the Asynchronous Status Register – ASSR has been implemented.

When entering Power-save or Extended Standby mode after having written to TCNT0, OCR0, or TCCR0, the user must wait until the written register has been updated if Timer/Counter0 is used to wake-up the device. Otherwise, the MCU will enter sleep mode before the changes are effective. This is particularly important if the Output Compare (OC0) interrupt is used to wake-up the device, since the output compare function is disabled during writing to OCR0 or TCNT0. If the write cycle is not finished, and the MCU awakens before the OCR0 or TCNT0 returns to zero, the device will never receive a compare match event, and the device will not wake up.

If Timer/Counter0 is used to wake the device up from Power-save or Extended Standby mode, precautions must be taken if the user wants to re-enter one of these modes. The interrupt logic needs one TOCKI cycle to be reset. If the time between wake-up and reentering is longer than one TOCKI cycle, the interrupt will not occur, and the device will fail to wake up. If the user is in doubt whether the time before re-entering Power-save or Extended Standby mode is sufficient, the following algorithm can be used to ensure that one TOCKI cycle has elapsed:

1. Write a value to TCCR0, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.
If Timer/Counter0 is used to wake the device up [...], precautions must be taken [...]

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2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.
If Timer/Counter0 is used to wake the device up […], precautions must be taken […]

1. Write a value to TCCRO, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.
If Timer/Counter0 is used to wake the device up [...], precautions must be taken [...]

1. Write a value to TCCR0, TCNT0, or OCR0.
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3. Enter Power-save or Extended Standby mode.

 specifications
ADP Example

ATmega128

- When writing to one of the registers TCNT0, OCR0, or TCCR0, the value is transferred to a temporary register, and latched after two positive edges on TOCN. The user should not write a new value before the contents of the Temporary Register have been transferred to its destination. Each of the three mentioned registers have their individual temporary registers, which means that e.g., writing to TCNT0 does not disturb an OCR0 write in progress. To detect that a transfer to the destination register has taken place, the Asynchronous Status Register — ASFR — has been implemented.

- When entering Power-save or Extended Standby mode after having written to TCNT0, OCR0, or TCCR0, the user need wait until the written register has been updated. If Timer/Counter0 is used to wake up the device, otherwise, the MCU will enter sleep mode before the changes are effective. This is particularly important if the Output Compare0 interrupt is used to wake up the device, since the output compare function is disabled during writing to OCR0 or TCNT0. If the write cycle is not finished, and the MCU enters sleep mode before the OCR0/TCNT0 returns to zero, the device will never receive a compare match event, and the MCU will not wake up.

- If Timer/Counter0 is used to wake the device up from Power-save or Extended Standby mode, precautions must be taken if the user wants to re-enter one of these modes. The interrupt logic needs one TOCN cycle to be reset. If the interrupt condition is reset before this, the interrupt will not occur, and the device will fail to wake up. If the user is in doubt whether the time before re-entering Power-save or Extended Standby mode is sufficient, the following algorithm can be used to ensure that one TOCN cycle has elapsed:

  1. Write a value to TCCR0, TCNT0, or OCR0.
  2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
  3. Enter Power-save or Extended Standby mode.
If Timer/Counter0 is used to wake the device up [...] precautions must be taken [...]

1. Write a value to TCCRO, TCNT0, or OCR0.
2. Wait until the corresponding Update Busy flag in ASSR returns to zero.
3. Enter Power-save or Extended Standby mode.
Part III

Abstractions
TinyOS is an open source OS developed by Berkeley.

- Mixture of preemptive and cooperative execution models.

1. Hardware interrupts can preempt execution at any time (if not masked).

2. Tasks are functions that are posted for being executed when the system is idle.
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- Mixture of preemptive and cooperative execution models.

1. Hardware interrupts can preempt execution at any time (if not masked).

2. Tasks are functions that are posted for being executed when system is idle.

Concrete Environment

\[ \mathcal{E} = M \times S \times Q \times I \]

- Memory
- HW state
- Tasks queue
- Interrupts
Hardware State Partitioning

Definition

- Hardware state is the primary information in the analysis.
- We should keep precise information about it.
- Memory content should be in relation with the hardware state because program infer the state by accessing hardware registers and/or some program variables.
Hardware State Partitioning

Definition

- Hardware state is the primary information in the analysis.
- We should keep precise information about it.
- Memory content should be in relation with the hardware state because program infer the state by accessing hardware registers and/or some program variables.

Hardware State Partitioning $\mathcal{D}_S$

1. First, we partition the environments w.r.t. automaton states $S$.
2. Then, we use a numerical abstract domain $\langle \mathcal{D}_\mathcal{M}, \sqsubseteq \mathcal{M} \rangle$ to abstract the values of registers and variables.

$$\langle \phi(\mathcal{E}), \sqsubseteq \rangle \leftrightarrow \langle S \rightarrow \mathcal{D}_\mathcal{M}, \dot{\sqsubseteq} \mathcal{M} \rangle$$
Hardware State Partitioning

Example

```c
void main() {
    // Config timer
    ...
    // Wait for interrupt
    while (1) {
        asm volatile("sleep");
        ...
    }
}

ISR(TIMER0_OVF_vect) {
    ... // Stabilize the timer
    TCCR0 = TCCR0;
    while (ASSR & 1 << TCR0UB);
    // Continue work
    ...
}
```

Diagram:

- **STABLE**
  - Transition on event `e:α` from `SLEEP`.
  - Transition on event `a:ASSR&=~(1<<TCROUB)` from `BUSY`.

- **BUSY**
  - Transition on event `e:sleep` from `SLEEP`.

- **SLEEP**
  - Transition on event `e:sleep` from `STABLE`.

- **UNSTBL**
  - Transition on event `e:sleep` from `BUSY`.

- **BUG**
  - Transition on event `e:TCCR0w` from `SLEEP`.
  - Transition on event `a:ASSR|(1<<TCROUB)` from `STABLE`.
  - Transition on event `e:int15|16` from `UNSTBL`.

Hardware State Partitioning

Example

```c
void main () {
    // Config timer
    ...
    // Wait for interrupt
    while (1) {
        asm volatile("sleep":);
        ...
    }
}

ISR (TIMER0_OVF_vect) {
    ...
    // Stabilize the timer
    TCCRO = TCCRO;
    while (ASSR & 1 << TCR0UB);
    // Continue work
    ...
}
```

```
<table>
<thead>
<tr>
<th>X6</th>
<th>X11</th>
<th>X14</th>
<th>X17</th>
</tr>
</thead>
</table>
```

```
| STABLE | BUSY   | SLEEP  | UNSTBL |

- e:α
  - a:ASSR&=(1<<TCROUB)
  - e:sleep

- e:sleep
  - e:TCCROw
  - a:ASSR|=(1<<TCROUB)

- e:sleep
  - e:int15|16
```
Hardware State Partitioning

Example

```c
1 void main() {
2    // Config timer
3    ...
4    // Wait for interrupt
5    while (1) {
6        asm volatile("sleep":);
7        ...
8    }
9 }
10 ISR(TIMER0_OVF_vect) {
11    ...
12    // Stabilize the timer
13    TCCR0 = TCCR0;
14    while
15        (ASSR & 1 << TCR0UB);
16    // Continue work
17    ...
18 }
```

Diagram:

```
+-------------------+                +-------------------+                +-------------------+                +-------------------+
| BUSY              |                | BUSY              |                | BUSY              |                | BUSY              |
| e:sleep           |                | e:sleep           |                | e:sleep           |                | e:sleep           |
| a:ASSR&=-1<<TCR0UB|                | a:ASSR&=-1<<TCR0UB|                | a:ASSR&=-1<<TCR0UB|                | a:ASSR&=-1<<TCR0UB|
| STABLE            |                | STABLE            |                | STABLE            |                | STABLE            |
| e:α               |                | e:α               |                | e:α               |                | e:α               |
| b:ASSR|=1<<TCR0UB  |                | b:ASSR|=1<<TCR0UB  |                | b:ASSR|=1<<TCR0UB  |                | b:ASSR|=1<<TCR0UB  |
+-------------------+                +-------------------+                +-------------------+                +-------------------+
```

<table>
<thead>
<tr>
<th></th>
<th>X_6</th>
<th>X_11</th>
<th>X_14</th>
<th>X_17</th>
</tr>
</thead>
<tbody>
<tr>
<td>STABLE</td>
<td>ASSR = 0</td>
<td>ASSR = 0</td>
<td>ASSR = 1</td>
<td>ASSR = 0</td>
</tr>
<tr>
<td>UNSTBL</td>
<td>ASSR = 0</td>
<td>ASSR = 0</td>
<td>ASSR = 0</td>
<td>ASSR = 0</td>
</tr>
<tr>
<td>BUSY</td>
<td>ASSR = 1</td>
<td>ASSR = 1</td>
<td>ASSR = 0</td>
<td>ASSR = 0</td>
</tr>
<tr>
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</tr>
</tbody>
</table>
Example: SPI serial transfer with a task polling (instead of an active polling).
Example: SPI serial transfer with a **task polling** (instead of an active polling).

```c
task void tx() {
    if (i < m_len) {
        SPDR = m_data[i];
        post check();
        return;
    }
    post end();
}
```

```c
task void check() {
    if !(SPSR &(1 << SPIF))
        post check();
    else {
        m_answer[i] = SPDR;
        i++;
        post tx();
    }
}
```

```c
task void end() {
    SPCR &= ~(1 << SPE);
    ...
}
```
Example: SPI serial transfer with a **task polling** (instead of an active polling).

```c
task void tx() {
    if (i < m_len) {
        SPDR = m_data[i];
        post check();
        return;
    } else {
        post end();
    }
}
```

```c
task void check() {
    if !(SPSR&(1<<SPIF))
        post check();
    else {
        m_answer[i] = SPDR;
        i++;
        post tx();
    }
}
```

```c
task void end() {
    SPCR &=~(1<<SPE);
    ...
}
```

**Rule**

Data register `SPDR` can not be used when the bus is not free.
We can not verify this ADP with $\mathcal{D}_S^\#$ since we consider every possible order of tasks.

We distinguish between the case when a task is posted or not.

We count the number of occurrences of posted tasks.

\[
\langle \rho(\mathcal{E}), \subseteq \rangle \iff \langle \rho(\mathcal{T}) \to (\mathcal{D}_S^\# \times \mathcal{N}_T^\#), \subseteq \rangle_Q
\]

- $\{tx\}$
  - ON
    - $i \in [0, m\_len]$ SPSR = 0
    - $tx = 1$
  - BUSY
    - $i \in [0, m\_len]$ SPSR = 0
    - $check = 1$
  - DONE
    - $i \in [0, m\_len]$ SPSR = 0x80
    - $check = 1$
  - $ON$
    - $i = m\_len$
    - $SPSR = 0$
    - $end = 1$

- $\emptyset$
  - OFF
    - $i = m\_len$
    - $SPSR = 0$
Abstraction of Preemption

Overview

Modular Preemption Analysis

- Avoid re-analyzing interrupts each time they are enabled.

```c
task void t() {
    SPCR |= (1<<SPE);
    ...
    x = y * i;
}
```

```c
ISR(ADC_vect) {
    ...
}
ISR(SPI_STC_vect) {
    ...
}
```
Abstraction of Preemption

Overview

Modular Preemption Analysis

- Avoid re-analyzing interrupts each time they are enabled.
- Collect the preemption environments at possible fire sites and analyze interrupts independently.

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Abstraction of Preemption

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Modular Preemption Analysis

- Avoid re-analyzing interrupts each time they are enabled.
- Collect the preemption environments at possible fire sites and analyze interrupts independently.
- The result environments are injected at fire sites to approximate the effect of interrupts.

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void t() {
    SPCR |= (1<<SPE);
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Abstraction of Preemption

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Modular Preemption Analysis

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```c
task void t() {
  SPCR |= (1<<SPE);
  ...
  x = y * i;
}
```

```c
ISR(ADC_vect)
{
  ...
}
```

```c
ISR(SPI_STC_vect)
{
  ...
}
```
Abstraction of Preemption

Definition

Abstraction of Interrupts Masks

\[ \mathcal{D}_K \triangleq \left\{ \perp_0, 0, 1, \top_0 \right\} \times \left( \varphi(\mathcal{I}) \to \mathcal{D}_Q \right) \]

- \( \mathcal{K}_G \) is an abstraction of the global interrupt flag. It is modified by statements like `asm volatile("sei": : :"memory")`.
- \( \mathcal{K}_P \) is a partitioning of environments w.r.t. active interrupts. It is affected by modification of specific hardware registers.
Abstraction of Preemption

Definition

Abstraction of Interrupts Masks

\[ D_K^k \triangleq \{ \bot_0, 0, 1, \top_1 \} \times (\wp(\emptyset) \rightarrow D_Q^k) \]

- \( K_G^k \) is an abstraction of the global interrupt flag. It is modified by statements like \texttt{asm volatile("sei":::"memory")}.

- \( K_P^k \) is a partitioning of environments w.r.t. active interrupts. It is affected by modification of specific hardware registers.

Abstraction of Interruption Environments

\[ D_I^k \triangleq D_K^k \times (\emptyset \rightarrow D_K^k) \times (\emptyset \rightarrow D_K^k) \]

Preemption \hspace{1cm} \text{Return}
Prototype implementation called SADA (*Static Analysis with Device Abstraction*).

Done in OCaml (~ 4000 lines of code).

Using CIL and Apron.

Seven ADPs were analyzed related to three devices:

1. Wireless transceiver CC2420.
2. Analog switch ADG715.
3. ATmega128 timer.

Two driver implementations for each device: TinyOS 1.x and 2.x.

- Very different design and algorithms.
- **Same property** can be used.
| Driver     | LoC  | # ISR | | T| | ADP       | | S| | $D_I^L(D_S^L)$ | | $D_I^L(D_Q^L)$ |
|------------|------|-------|---|---|------------|---|---|----------------|----------------|
| CC2420 1.x | 2666 | 1     | 1 |   | $A_{SPI-SS}$ | 4 | 12  | 12 ✓          | 850 42 ✓        |
|            |      |       |   |   | $A_{SPI-TX}$  | 10| 21  | 13 ✓          | 1600 74 ✓       |
| CC2420 2.x | 10133| 2     | 10|   | $A_{SPI-SS}$  | 4 | $\infty$ | 34 18 ✓        | 39 18 ✓        |
|            |      |       |   |   | $A_{SPI-TX}$  | 10| $\infty$ | 34 18 ✓        | 39 18 ✓        |
| ADG715 1.x | 2038 | 1     | 1 |   | $A_{PULL-UP}$ | 4 | 1  | 11 x          | 1 11 x         |
|            |      |       |   |   | $A_{TWI-TX}$  | 6 | 4  | 11 ✓          | 7 12 ✓         |
| ADG715 2.x | 4412 | 1     | 6 |   | $A_{PULL-UP}$ | 4 | 23 | 14 ✓          | 8 13 ✓         |
|            |      |       |   |   | $A_{TWI-TX}$  | 6 | 40 | 16 x          | 6 14 x         |
| Timer 1.x  | 1627 | 1     | 3 |   | $A_{STBL}$    | 7 | 6  | 11 x          | 39 16 x        |
|            |      |       |   |   | $A_{OCR0}$    | 4 | 3  | 10 x          | 29 15 x        |
|            |      |       |   |   | $A_{TCCR0}$   | 4 | 3  | 10 ✓          | 37 16 ✓        |
| Timer 2.x  | 2384 | 2     | 2 |   | $A_{STBL}$    | 4 | 7  | 12 ✓          | 26 13 ✓        |
|            |      |       |   |   | $A_{OCR0}$    | 4 | 10 | 12 ✓          | 38 13 ✓        |
|            |      |       |   |   | $A_{TCCR0}$   | 4 | 10 | 11 x          | 23 13 x        |
## Experiments

### Results

<p>| Driver      | LoC  | # ISR | T | ADP   | |S| | (D_T(D_S)) | (D_T(D_Q)) |
|-------------|------|-------|---|-------|---|---|----------------|----------------|
| CC2420 1.x  | 2666 | 1     | 1 | (\mathcal{A}<em>{SPI-ss}) | 4 | 12 | ✔️ | 850 | ✔️ |
|             |      |       |   | (\mathcal{A}</em>{SPI-tx}) | 10| 21 | ✔️ | 1600| ✔️ |
| CC2420 2.x  | 10133| 2     | 10| (\mathcal{A}<em>{SPI-ss}) | 4 | ∞  | ✔️ | 34  | ✔️ |
|             |      |       |   | (\mathcal{A}</em>{SPI-tx}) | 10| ∞  | ✔️ | 39  | ✔️ |
| ADG715 1.x  | 2038 | 1     | 1 | (\mathcal{A}<em>{pull-up}) | 4 | 1  | ✗  | 1   | ✗  |
|             |      |       |   | (\mathcal{A}</em>{TWI-tx}) | 6 | 4  | ✔️ | 7   | ✔️ |
| ADG715 2.x  | 4412 | 1     | 6 | (\mathcal{A}<em>{pull-up}) | 4 | 23 | ✔️ | 8   | ✔️ |
|             |      |       |   | (\mathcal{A}</em>{TWI-tx}) | 6 | 40 | ✗  | 6   | ✗  |
| Timer 1.x   | 1627 | 1     | 3 | (\mathcal{A}<em>{STBL})   | 7 | 6  | ✗  | 39  | ✗  |
|             |      |       |   | (\mathcal{A}</em>{OCR0})   | 4 | 3  | ✗  | 29  | ✗  |
|             |      |       |   | (\mathcal{A}<em>{TCCR0})  | 4 | 3  | ✔️ | 37  | ✔️ |
| Timer 2.x   | 2384 | 2     | 2 | (\mathcal{A}</em>{STBL})   | 4 | 7  | ✔️ | 26  | ✔️ |
|             |      |       |   | (\mathcal{A}<em>{OCR0})   | 4 | 10 | ✔️ | 38  | ✔️ |
|             |      |       |   | (\mathcal{A}</em>{TCCR0})  | 4 | 10 | ✗  | 23  | ✗  |</p>
<table>
<thead>
<tr>
<th>Driver</th>
<th>LoC</th>
<th># ISR</th>
<th></th>
<th></th>
<th>ADP</th>
<th></th>
<th></th>
<th>$D_T^I(D_S^II)$</th>
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<tr>
<td>CC2420 1.x</td>
<td>2666</td>
<td>1</td>
<td>1</td>
<td></td>
<td>$A_{SPI-ss}$</td>
<td>4</td>
<td>12</td>
<td>12</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{SPI-tx}$</td>
<td>10</td>
<td>21</td>
<td>13</td>
<td>✓</td>
</tr>
<tr>
<td>CC2420 2.x</td>
<td>10133</td>
<td>2</td>
<td>10</td>
<td></td>
<td>$A_{SPI-ss}$</td>
<td>4</td>
<td></td>
<td>∞</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{SPI-tx}$</td>
<td>10</td>
<td></td>
<td>∞</td>
<td></td>
</tr>
<tr>
<td>ADG715 1.x</td>
<td>2038</td>
<td>1</td>
<td>1</td>
<td></td>
<td>$A_{PULL-up}$</td>
<td>4</td>
<td>1</td>
<td>11</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{TWI-tx}$</td>
<td>6</td>
<td>4</td>
<td>11</td>
<td>✓</td>
</tr>
<tr>
<td>ADG715 2.x</td>
<td>4412</td>
<td>1</td>
<td>6</td>
<td></td>
<td>$A_{PULL-up}$</td>
<td>4</td>
<td>23</td>
<td>14</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{TWI-tx}$</td>
<td>6</td>
<td>40</td>
<td>16</td>
<td>✗</td>
</tr>
<tr>
<td>Timer 1.x</td>
<td>1627</td>
<td>1</td>
<td>3</td>
<td></td>
<td>$A_{STBL}$</td>
<td>7</td>
<td>6</td>
<td>11</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{OCR0}$</td>
<td>4</td>
<td>3</td>
<td>10</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{TCCR0}$</td>
<td>4</td>
<td>3</td>
<td>10</td>
<td>✓</td>
</tr>
<tr>
<td>Timer 2.x</td>
<td>2384</td>
<td>2</td>
<td>2</td>
<td></td>
<td>$A_{STBL}$</td>
<td>4</td>
<td>7</td>
<td>12</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{OCR0}$</td>
<td>4</td>
<td>10</td>
<td>12</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$A_{TCCR0}$</td>
<td>4</td>
<td>10</td>
<td>11</td>
<td>✗</td>
</tr>
</tbody>
</table>
## Experiments

### Results

| Driver       | LoC  | # ISR | # | ADP      | |S| | $D^H_I(D^H_S)$ | $D^H_I(D^H_Q)$ |
|--------------|------|-------|---|----------|---|---|----------------|----------------|
| CC2420 1.x   | 2666 | 1     | 1 | $A_{SPI-ss}$ | 4 | 12 | 12  | ✓             | ✓             |
|              |      |       |   | $A_{SPI-tx}$ | 10| 21 | 13  | ✓             | ✓             |
| CC2420 2.x   | 10133| 2     | 10| $A_{SPI-ss}$ | 4 | ∞  |      | ✓             | ✓             |
|              |      |       |   | $A_{SPI-tx}$ | 10| ∞  |      | ✓             | ✓             |
| ADG715 1.x   | 2038 | 1     | 1 | $A_{pull-up}$ | 4 | 1  | 11  | ×             | ×             |
|              |      |       |   | $A_{TWI-tx}$ | 6 | 4  | 11  | ✓             | ✓             |
| ADG715 2.x   | 4412 | 1     | 6 | $A_{pull-up}$ | 4 | 23 | 14  | ✓             | ✓             |
|              |      |       |   | $A_{TWI-tx}$ | 6 | 40 | 16  | ×             | ×             |
| Timer 1.x    | 1627 | 1     | 3 | $A_{STBL}$ | 7 | 6  | 11  | ☐            | ☐            |
|              |      |       |   | $A_{OCR0}$ | 4 | 3  | 10  | ☐            | ☐            |
|              |      |       |   | $A_{TCCR0}$ | 4 | 3  | 10  | ✓             | ✓             |
| Timer 2.x    | 2384 | 2     | 2 | $A_{STBL}$ | 4 | 7  | 12  | ✓             | ✓             |
|              |      |       |   | $A_{OCR0}$ | 4 | 10 | 12  | ✓             | ✓             |
|              |      |       |   | $A_{TCCR0}$ | 4 | 10 | 11  | ×             | ×             |
## Related Work

<table>
<thead>
<tr>
<th>Approach</th>
<th>Tool</th>
<th>Properties</th>
<th>Preemption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic analysis</td>
<td>SafeTinyOS</td>
<td>Runtime</td>
<td>Enumeration</td>
</tr>
<tr>
<td></td>
<td>TemporalMonitors</td>
<td>Runtime/LTL</td>
<td></td>
</tr>
<tr>
<td>Model checking</td>
<td>TOS2CProver</td>
<td>Runtime</td>
<td>Sequenlization</td>
</tr>
<tr>
<td></td>
<td>i-CBMC</td>
<td>Runtime</td>
<td>Partial order encoding</td>
</tr>
<tr>
<td>Deductive methods</td>
<td>[Duan &amp; Regeher]</td>
<td>Hardware</td>
<td>Not supported</td>
</tr>
<tr>
<td>Abstract interpretation</td>
<td>[Monniaux]</td>
<td>Hardware</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MCSquare</td>
<td>Runtime</td>
<td>Sequenlization</td>
</tr>
<tr>
<td></td>
<td>[Wu et al.]</td>
<td>Runtime</td>
<td></td>
</tr>
</tbody>
</table>
An abstract interpreter for verifying *hardware interactions* in TinyOS device drivers was presented.

It is based on different levels of partitioning for handling hardware state, tasks queue and interrupt masks.

Preemption is formalized using an iterative and modular fixpoint analysis.

Future Work

- Develop abstract domains for timing specifications of devices.
- Consider other cooperative models (e.g. Protothreads of Contiki).